IDEC Chip Design Contest

Sub-6 GHz switch and LNA design

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• Introduction

- ✓ SPDT switch and LNA fabricated using a 28-nm CMOS fabrication
- ✓ Designed for Sub-6 GHz for 5G Application
- ✓ The SPDT switch is designed with low insertion loss (<1dB*) and high isolation (>45dB*)
- ✓ The LNA is designed with resistive feedback and buffer stage matching for broadband
- ✓ The LNA achieved higher than 20 dB* of gain and less than 3 dB*

* Simulation data

• Description

◆ Schematic of Switch [Fig.1]

- ✓ To reduce insertion loss and increase isolation, series / shunt configuration is used.
- ✓ The width of series / shunt transistors is optimized by trade-off relationship between insertion loss and isolation.
- ✓ To increase power handling capability, stacked topology is used to increase maximum output voltage limitation.
- ✓ To reduce insertion loss, RF floating resistor is used in gate and body.
- ✓ To increase power handling capability, negative bias is used in gate and body.

◆ Schematic of LNA [Fig.2]

- ✓ To obtain high gain and low noise characteristics, the cascode topology is adopted for LNA structure.
- ✓ To obtain input matching and noise figure matching simultaneously, the degeneration inductor is used.
- ✓ Resistive feed back structure is used to achieve the broadband characteristic.
- ✓ Since passive components limit the frequency band, the proposed LNA replaces the passive components with a buffer stage that is ideally independent of frequency.

◆ Layout of SPDT Switch [Fig.3]

- ✓ Considering that the transistor cannot be rotated, the series and shunt branches are designed.
- ✓ The MMIC was designed with RF and DC PAD to measure with the probe.

◆ Layout of LNA [Fig.4]

- ✓ Since the target frequency is sub-6GHz and this frequency is low, the large size inductors are used to matching and inductive load.
- ✓ To prevent oscillation, the bypass capacitor is used at remaining area.

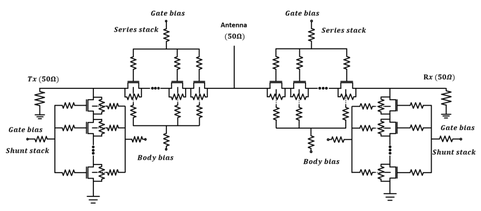

Fig. 1. Schematic of Switch

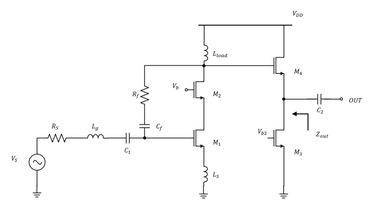

Fig. 2. Schematic of LNA

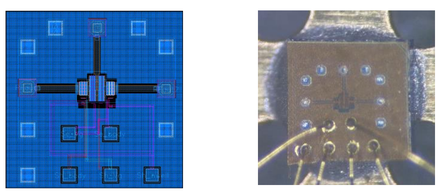

Fig. 3. Layout and Fabrication of Switch

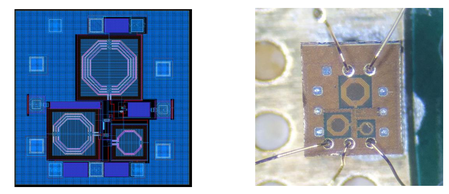

Fig. 4. Layout and Fabrication of LNA

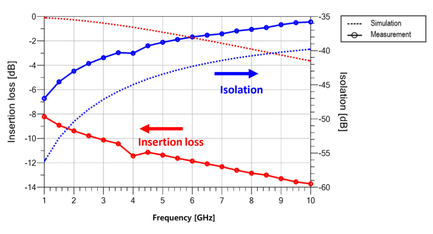

Fig. 5. Simulation and Measurement of Switch

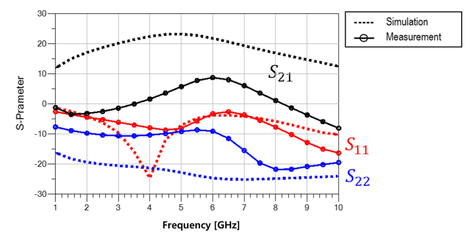

Fig. 6. Simulation and Measurement of LNA

• Conclusion

- ✓ LNA and SPDT switch is designed for 5G application
- ✓ LNA chip verification was not done properly due to the oscillation of the buffer amplifier
- ✓ Switch was not sufficiently considered of gate tie-down and backside condition
- ✓ It is necessary to consider the effect of parasitic components, backside substrate and gate tie-down diode for next design.

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